

Applications of Formal Verification

Model Checking: Introduction to SPIN

Prof. Dr. Bernhard Beckert · Dr. Vladimir Klebanov | SS 2012



SPIN: Previous Lecture vs. This Lecture



Previous lecture

SPIN appeared as a PROMELA simulator

This lecture

Intro to SPIN as a model checker



A Model Checker (MC) is designed to prove the user wrong.

MC tries its best to *find a counter example* to the correctness properties.

It is tuned for that.

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MC's search for counter examples is exhaustive.

⇒ Finding no counter example proves stated correctness properties.

What does 'exhaustive search' mean here?



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=

resolving non-determinism in all possible ways

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resolving non-determinism in all possible ways

For model checking PROMELA code, two kinds of non-determinism to be resolved:

explicit, local: if/do statements

```
:: guardX -> ....
:: guardY -> ....
```

 implicit, global: scheduling of concurrent processes (see next lecture)



SPIN: "Simple Promela Interpreter"



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Main functionality of SPIN:

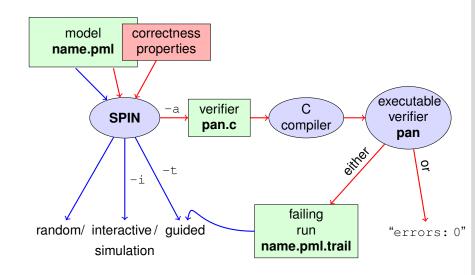
- simulating a model (randomly/interactively/guided)
- generating a verifier

verifier generated by SPIN is a C program performing model checking:

- exhaustively checks PROMELA model against correctness properties
- in case the check is negative: generates a failing run of the model, to be simulated by SPIN

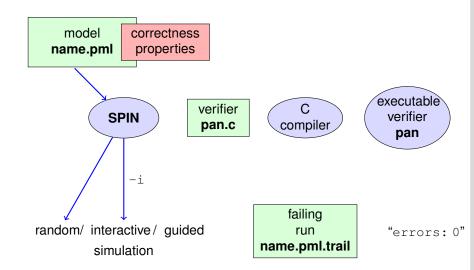
SPIN Workflow: Overview





Plain Simulation with SPIN





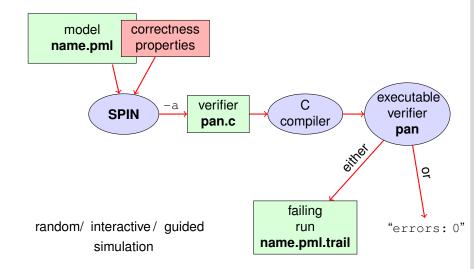
Rehearsal: Simulation Demo



run example, random and interactive interleave.pml, zero.pml

Model Checking with SPIN





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Meaning of Correctness wrt. Properties



Given PROMELA model M, and correctness properties C_1, \ldots, C_n .

- Be R_M the set of all possible runs of M.
- For each correctness property C_i , R_{M,C_i} is the set of all runs of M satisfying C_i . $(R_{M,C_i} \subseteq R_M)$
- M is correct wrt. C_1, \ldots, C_n iff $(R_{M,C_1} \cap \ldots \cap R_{M,C_n}) = R_M$.
- If M is not correct, then each $r \in (R_M \setminus (R_{M,C_1} \cap ... \cap R_{M,C_n}))$ is a counter example.

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We know how to write models M.

Meaning of Correctness wrt. Properties

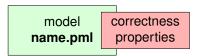


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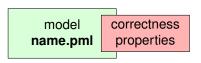
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We know how to write models *M*. But how to write Correctness Properties?



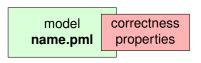






Correctness properties can be stated (syntactically) within or outside the model.



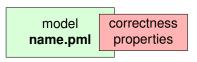


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stating properties within the model, using

assertion statements





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- assertion statements
- meta labels
 - end labels
 - accept labels
 - progress labels



model correctness properties

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stating properties outside the model, using

- never claims
- temporal logic formulas



model correctness properties

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- assertion statements (today)
- meta labels
 - end labels (today)
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Definition (Assertion Statements)

Assertion statements in PROMELA are statements of the form assert(expr)

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stmt1;
assert(max == a);
stmt2;
...
```



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Typically, expr is of type bool.

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```
...
stmt1;
assert(max == a);
stmt2;
...
if
:: b1 -> stmt3;
assert(x < y)
:: b2 -> stmt4
```

Meaning of Boolean Assertion Statements



assert(EXDT)

- has no effect if expr evaluates to true
- triggers an error message if expr evaluates to false

This holds in both, simulation and model checking mode.

Meaning of General Assertion Statements



assert (expr)

- has no effect if expr evaluates to non-zero value
- triggers an error message if expr evaluates to 0

This holds in both, simulation and model checking mode.

Meaning of General Assertion Statements



assert(*expr*)

- has no effect if expr evaluates to non-zero value
- triggers an error message if expr evaluates to 0

This holds in both, simulation and model checking mode.

Recall:

bool true false is syntactic sugar for

Meaning of General Assertion Statements



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Recall:

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```

Meaning of General Assertion Statements



assert(*expr*)

- has no effect if expr evaluates to non-zero value
- triggers an error message if expr evaluates to 0

This holds in both, simulation and model checking mode.

Recall:

```
bool true false is syntactic sugar for bit 1 	 0
```

⇒ general case covers Boolean case

Instead of using 'printf's for Debugging ...



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Command Line Execution

(simulate, inject faults, add assertion, simulate again)

```
> spin max.pml
```

... we can employ Assertions



quoting from file max.pml:

```
/* after choosing a,b from {1,2,3} */
if
    :: a >= b -> max = a;
    :: a <= b -> max = b;
fi;
assert( a > b -> max == a : max == b )
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... we can employ Assertions



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Now, we have a first example with a formulated correctness property.

... we can employ Assertions



quoting from file max.pml:

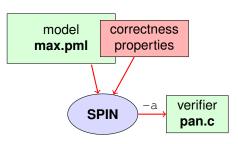
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Now, we have a first example with a formulated correctness property.

We can do model checking, for the first time!

Generate Verifier in C





Command Line Execution

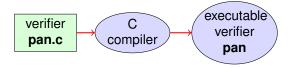
Generate Verifier in C

> spin -a max.pml

SPIN generates Verifier in C, called pan.c (plus helper files)

Compile To Executable Verifier





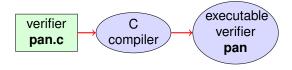
Command Line Execution

compile to executable verifier

> gcc -o pan pan.c

Compile To Executable Verifier





Command Line Execution

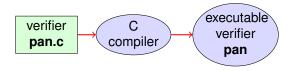
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C compiler generates executable verifier pan

Compile To Executable Verifier





Command Line Execution

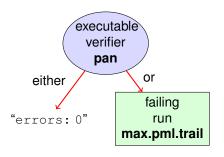
compile to executable verifier

> gcc -o pan pan.c

C compiler generates executable verifier pan

pan: historically "protocol analyzer", now "process analyzer"

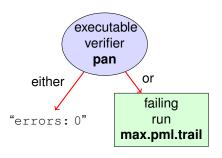




Command Line Execution

run verifier pan





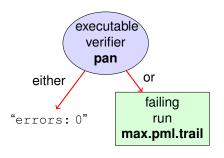
Command Line Execution

run verifier **pan**

> ./pan

prints "errors: 0"





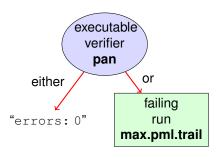
Command Line Execution

run verifier **pan**

> ./pan

■ prints "errors: 0" ⇒ Correctness Property verified!



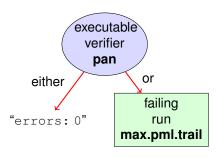


Command Line Execution

run verifier pan

- prints "errors: 0", or
- prints "errors: n" (n > 0)



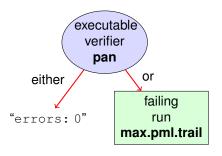


Command Line Execution

run verifier **pan**

- prints "errors: 0", or
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Command Line Execution

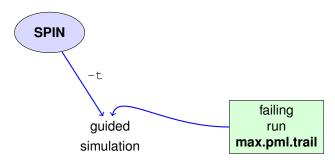
run verifier pan

- prints "errors: 0", or
- prints "errors: n" (n > 0) \Rightarrow counter example found! records failing run in max.pml.trail

Guided Simulation



To examine failing run: employ simulation mode, "guided" by trail file.



Command Line Execution

inject a fault, re-run verification, and then:

Output of Guided Simulation



can look like:

Output of Guided Simulation



can look like:

assignments in the run

Output of Guided Simulation



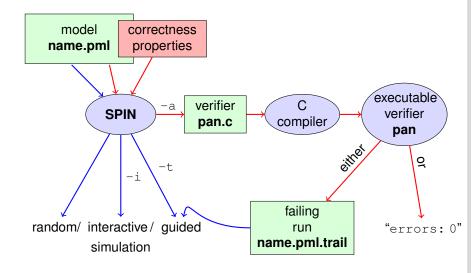
can look like:

assignments in the run values of variables whenever updated

What did we do so far?



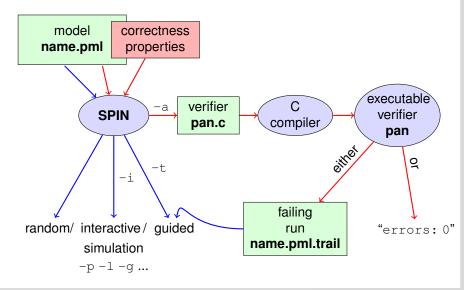
following whole cycle (most primitive example, assertions only)



What did we do so far?



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Further Examples: Integer Division



```
int dividend = 15;
int divisor = 4;
int quotient, remainder;
quotient = 0;
remainder = dividend;
do
  :: remainder > divisor ->
     quotient++;
     remainder = remainder - divisor
  :: else ->
     break
od;
printf("%d divided by %d = %d, remainder = %d\n",
       dividend, divisor, quotient, remainder);
```

Further Examples: Integer Division



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       break
  od;
  printf("%d divided by %d = %d, remainder = %d\n",
         dividend, divisor, quotient, remainder);
simulate, put assertions, verify, change values, ...
```



```
int x = 15, y = 20;
int a, b;
a = x; b = y;
do
   :: a > b -> a = a - b
   :: b > a -> b = b - a
   :: a == b -> break
od;
printf("The GCD of %d and %d = %d\n", x, y, a)
```



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full functional verification not possible here (why?) still, assertions can perform sanity check

⇒ typical for model checking



typical command line sequences: random simulation spin name.pml



typical command line sequences:

random simulation

spin name.pml

interactive simulation

spin -i name.pml



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typical command line sequences:
```

random simulation

spin name.pml

interactive simulation

spin -i name.pml

model checking

spin -a name.pml
gcc -o pan pan.c
./pan

and in case of error

spin -t -p -l -g name.pml

SPIN Reference Card



Ben-Ari produced Spin Reference Card, summarizing

- typical command line sequences
- options for
 - SPIN
 - gcc
 - pan
- PROMELA
 - datatypes
 - operators
 - statements
 - guarded commands
 - processes
 - channels
- temproal logic syntax

Why SPIN?



- SPIN targets software, instead of hardware verification
- \blacksquare based on standard theory of $\omega\text{-automata}$ and linear temporal logic
- 2001 ACM Software Systems Award (other winning software systems include: Unix, TCP/IP, WWW, TcI/Tk, Java)
- used for safety critical applications
- distributed freely as research tool, well-documented, actively maintained, large user-base in academia and in industry
- annual SPIN user workshops series held since 1995

Why SPIN? (Cont'd)



- PROMELA and SPIN are rather simple to use
- good to understand a few system really well, rather than many systems poorly
- availability of good course book (Ben-Ari)
- availability of front end JSPIN (also Ben-Ari)

What is JSPIN?



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- developed for pedagogical purposes
- written in Java
- simple user interface
- SPIN options automatically supplied
- fully configurable
- supports graphics output of transition system

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- graphical user interface for SPIN
- developed for pedagogical purposes
- written in Java
- simple user interface
- SPIN options automatically supplied
- fully configurable
- supports graphics output of transition system
- makes back-end calls transparent

JSPIN **Demo**



Command Line Execution

calling JSPIN

> java -jar /usr/local/jSpin/jSpin.jar
(with path adjusted to your setting)
or use shell script:

> jspin

JSPIN **Demo**



Command Line Execution

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play around with similar examples ...



quoting from file max2.pml:



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simulate a few times



quoting from file max2.pml:

simulate a few times

 \Rightarrow crazy "timeout" message sometimes



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generate and execute pan



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⇒ reports "errors: 1"
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quoting from file max2.pml:

simulate a few times

 \Rightarrow crazy "timeout" message sometimes

generate and execute pan

⇒ reports "errors: 1"

Note: no assert in max2.pml.



Further inspection of pan output:

```
pan: invalid end state (at depth 1)
pan: wrote max2.pml.trail
```



A process may legally block, as long as some other process can proceed.

32/34



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Blocking for letting others proceed is useful, and typical, for concurrent and distributed models (i.p. protocols).



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⇒ "Deadlock"



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Blocking for letting others proceed is useful, and typical, for concurrent and distributed models (i.p. protocols).

But

it's an error if a process blocks while no other process can proceed

 \Rightarrow "Deadlock"

in **max1.pml**, no process can take over.



Definition (Valid End State)

An end state of a run is valid iff the location counter of each processes is at an end location.



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- P's textual end
- each location marked with an end label: "endxxx:"

End labels are not useful in **max1.pml**, but elsewhere, they are. Example: end.pml

Literature for this Lecture



Ben-Ari Chapter 2, Sections 4.7.1, 4.7.2