Karlsruher Institut für Technologie

Synthesis of Beyond CMOS Reconfigurable Architectures

For decades, reconfigurable systems based on SRAM dominated the landscape of digital design, particularly in FPGAs. These SRAM-based architectures offered a significant degree of flexibility, enabling rapid prototyping and iterative design processes. However, as the limits of scaling, power consumption, and volatility began to surface with conventional CMOS technologies, researchers and industry pioneers started to explore alternatives that could transcend these inherent limitations.

Today, we are witnessing the emergence of reconfigurable systems that push beyond the boundaries of traditional CMOS. Among these new paradigms are architectures such as DPQA and NV-FPGA. DPQA represents an innovative approach that departs from the conventional SRAM-centric design, potentially harnessing unconventional circuit designs and device physics to deliver enhanced energy efficiency and greater integration density. Similarly, NV-FPGA leverages non-volatile memory elements to maintain configuration data even in the absence of power. This characteristic not only leads to reduced static power consumption but also significantly shortens power-up times, thereby increasing system reliability and offering unique operational advantages in dynamic environments.

The shift to these beyond CMOS systems is driven by a confluence of factors. Emerging device technologies—such as phase-change memory, spintronics, and other novel memory elements—offer promising benefits in terms of speed, energy efficiency, and endurance compared to traditional volatile memory components. These new materials and mechanisms open the door to architectures that are not solely defined by the limits of charge-based storage, thereby enabling a new generation of reconfigurable systems that operate under different physical principles.

One of the most compelling challenges accompanying this shift lies in the development of advanced synthesis tools. Traditional synthesis methodologies have been finely tuned to the predictable behavior of CMOS and SRAM-based devices. In contrast, beyond CMOS architectures introduce new device-level constraints such as variability, non-volatility, and unconventional switching behaviors. Consequently, synthesis tools must evolve to encapsulate these factors—integrating device physics models and heterogeneous design trade-offs into the toolchain. Researchers are now focusing on creating automated workflows that not only translate high-level design specifications into hardware configurations but also optimize for the nuanced performance, power, and reliability parameters characteristic of DPQA, NV-FPGA, and similar emerging architectures.

This ongoing development of specialized synthesis tools represents a critical frontier in the field. By directly addressing the challenges posed by new materials and emerging architectures, these tools aim to bridge the gap between theoretical device innovations and practical, deployable reconfigurable systems. As such, the synthesis of beyond CMOS architectures is not merely an incremental improvement—it is a comprehensive rethinking of the design automation process that is expected to redefine the standards of reconfigurable computing for the next generation.

To conclude, while SRAM-based reconfigurable systems have long been the workhorses of digital reconfigurability, the advent of DPQA and NV-FPGA signals a transformative shift toward beyond CMOS architectures. This synthesis lays the groundwork for integrating these innovations into mainstream design practices through advanced synthesis tools, ensuring that the full potential of next-generation reconfigurable technologies can be realized in future computing systems.

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